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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,498	10/08/2003	Martin Perner	P2002,0856	5905

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EXAMINER	
NGUYEN, HOAI AN D	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,498	PERNER, MARTIN	
	Examiner	Art Unit	
	Hoai-An D. Nguyen	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Wheless, JR et al. (US 2004/0236534 A1).

Wheless, JR et al. teach an integrated circuit with configuration based on parameter measurement comprising:

With regard to claims 1, 11, 12 and 19, a circuit configuration (FIG. 2, measurement circuit 28) for measuring at least one operating parameter for an integrated circuit (FIG. 1, integrated circuit 20), comprising: a counter circuit (FIG. 2, counters included in each gated counter measurement devices 28a-28d) logging at least one digitally coded value (counts) characterizing at least one operating parameter for specifying a mode of operation for the integrated circuit (Paragraphs [0034], [0040] and [0041]), an analysis circuit (FIG. 2, gated counter measurement devices 28a-28d) to be connected to at least one external connection (FIG. 1, system bus 38) on the integrated circuit (FIG. 1, integrated circuit 20), said analysis circuit detecting a plurality of voltage level changes (picking up start and stop bit patterns) on the external connection and supplying the voltage level changes to said counter circuit (Paragraphs

[0020] and [0050]), and an output circuit (FIG. 1, control circuit 22) connected to said analysis circuit (FIG. 2, gated counter measurement devices 28a-28d), said output circuit externally outputting said at least one digitally coded value or a value derived therefrom (Paragraphs [0025]-[0030] and [0040]).

With regard to claim 2, the external connection (FIG. 1, system bus 38) is used to control a method of operation for the integrated circuit (Paragraph [0023]).

With regard to claim 3, the counter circuit (FIG. 2, counter included in the gated counter measurement device 28d) logs the voltage level changes (picking up start and stop bit patterns) over a defined period of time (the length of the gated period) (Paragraph [0050]).

With regard to claims 4 and 13, the analysis circuit (FIG. 2, gated counter measurement devices 28a-28d) is to be connected to a plurality of external connections (FIG. 2, measurement paths 50a-50c) on the integrated circuit (Paragraph [0036]), and said counter circuit (FIG. 2, counters included in each gated counter measurement devices 28a-28d) has a combinational logic circuit (FIG. 2, gating logic, included in each gated counter measurement devices 28a-28d, connected to logic blocks 24a-24c) and is connected to the external connections through said combinational logic circuit (Paragraph [0040]).

With regard to claims 5, 6 and 14, the counter circuit (FIG. 2, counters included in each gated counter measurement devices 28a-28d) has combinational logic circuits (FIG. 2, gating logic, included in each gated counter measurement devices 28a-28d, connected to logic blocks 24a-24c), said analysis circuit (FIG. 2, gated counter measurement devices 28a-28d) is to be connected to a plurality of external connections (FIG. 2, measurement paths 50a-50c) on the integrated circuit (Paragraph [0036]) and has a plurality of counter circuits (FIG. 2, counters

included in each gated counter measurement devices 28a-28d), and each of said counter circuits to be connected to at least one the external connections through a different one of said combinational logic circuits (FIG. 2, gating logic, included in each gated counter measurement devices 28a-28d, connected to logic blocks 24a-24c) (Paragraphs [0039]-[0040]) and respectively logs at least one digitally coded value (Paragraphs [0046]-[0050]).

With regard to claim 7, the combinational logic circuit is one of hardwired and variably programmable (programmable) (Paragraph [0074]).

With regard to claims 8 and 9, the counter circuit is a plurality of counter circuits (FIG. 2, counters included in each gated counter measurement devices 28a-28d), and each of said counter circuits has an associated register to which a content of a respective associated one of said counter circuits is copied and stored (Paragraphs [0046]-[0050]). Noted that each counter can be reset and incremented, so they must have a memory storage or a register to store the current count value or a default value when reset.

With regard to claim 10, the analysis circuit has a time counter circuit connected to a clock signal connection for logging a defined period of time (Paragraphs [0041]-[0042]).

With regard to claims 15, 16 and 17, averaging the coded value or the value derived from the coded value (Paragraphs [0043]-[0044]).

With regard to claim 18, upon reaching an averaging time (the length of the gated period) that is a binary multiple during a measurement, relating the respective coded value logged up until the averaging time to the averaging time (Paragraphs [0042]-[0043]).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's attention is invited to the followings whose inventions disclose similar devices.

- Runas et al. (US 5,592,077 A) teach circuits, systems and methods for testing ASIC and RAM memory devices.
- Lawrence et al. (US 5,914,902 A) teach a synchronous memory tester.
- Cole, Jr. et al. (US 6,549,022 B1) teach an apparatus and method for analyzing functional failures in integrated circuits.
- Mori et al. (US 6,690,189 B2) teach an apparatus and method for testing semiconductor integrated circuit.
- Rickes et al. (US 6,714,469 B2) teach an on-chip compression of charge distribution data.
- Ainspan et al. (US 2004/0136436 A1) teach a digital measuring system and method for integrated circuit chip operating parameters.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai-An D. Nguyen whose telephone number is 571-272-2170. The examiner can normally be reached on M-F (8:00 - 5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANJAN DEB
PRIMARY EXAMINER

Hoai-An D. Nguyen
Examiner
Art Unit 2858
HADN

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